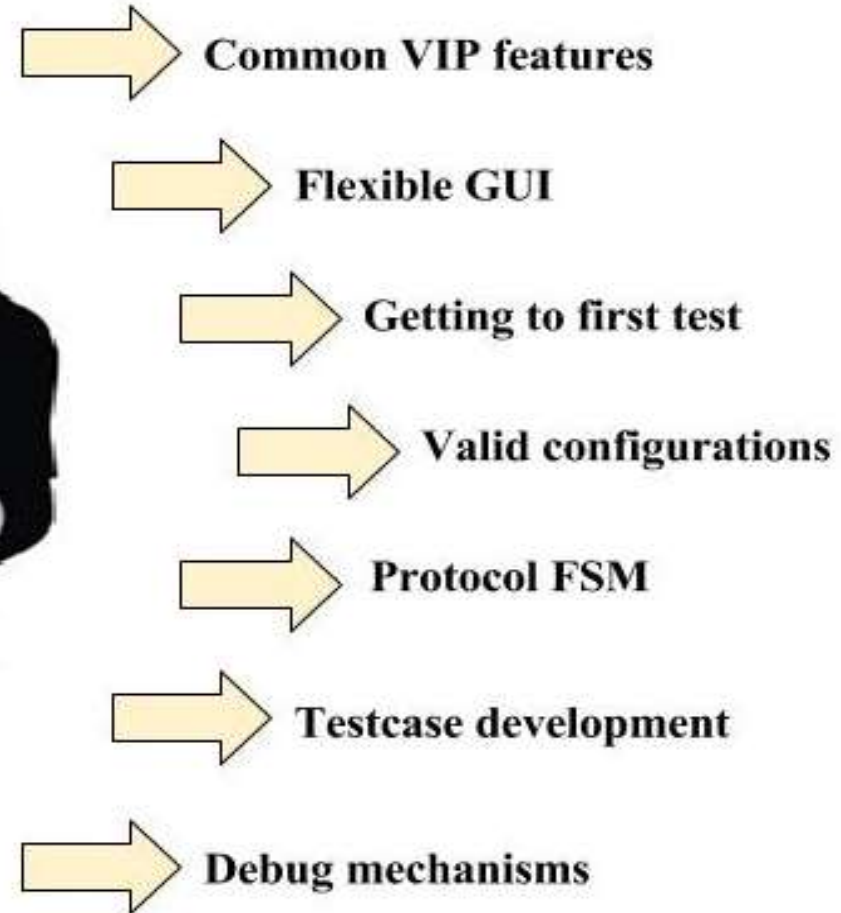# Technical aspects in choosing Verification Intellectual Property (VIP)
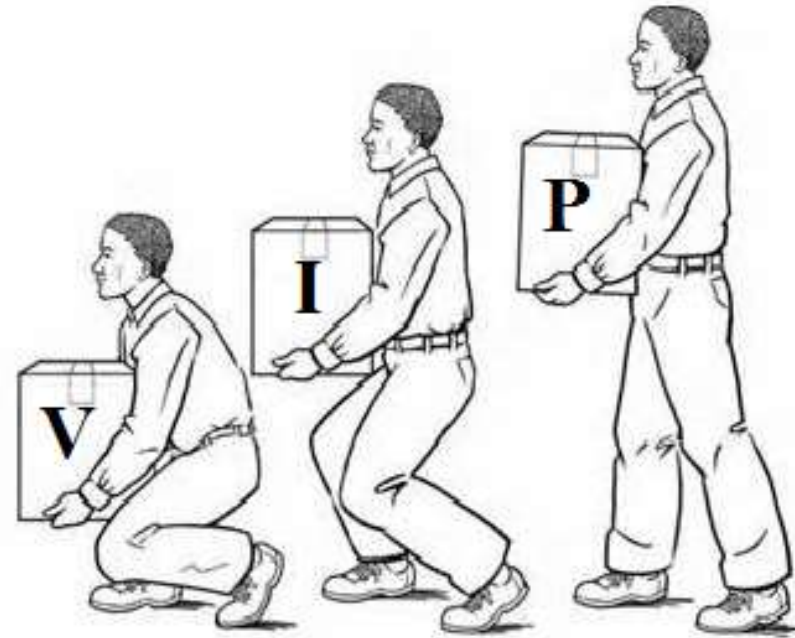
Mahesh K
Verification Engineer,
Innovative Logic Design Services Pvt Ltd,
Bangalore

Agenda

❏ Multiple benefits of VIP in a more productive way for complete IP and SOC verification.

Common VIP features

Flexible GUI

Getting to first test

Valid configurations

Protocol FSM

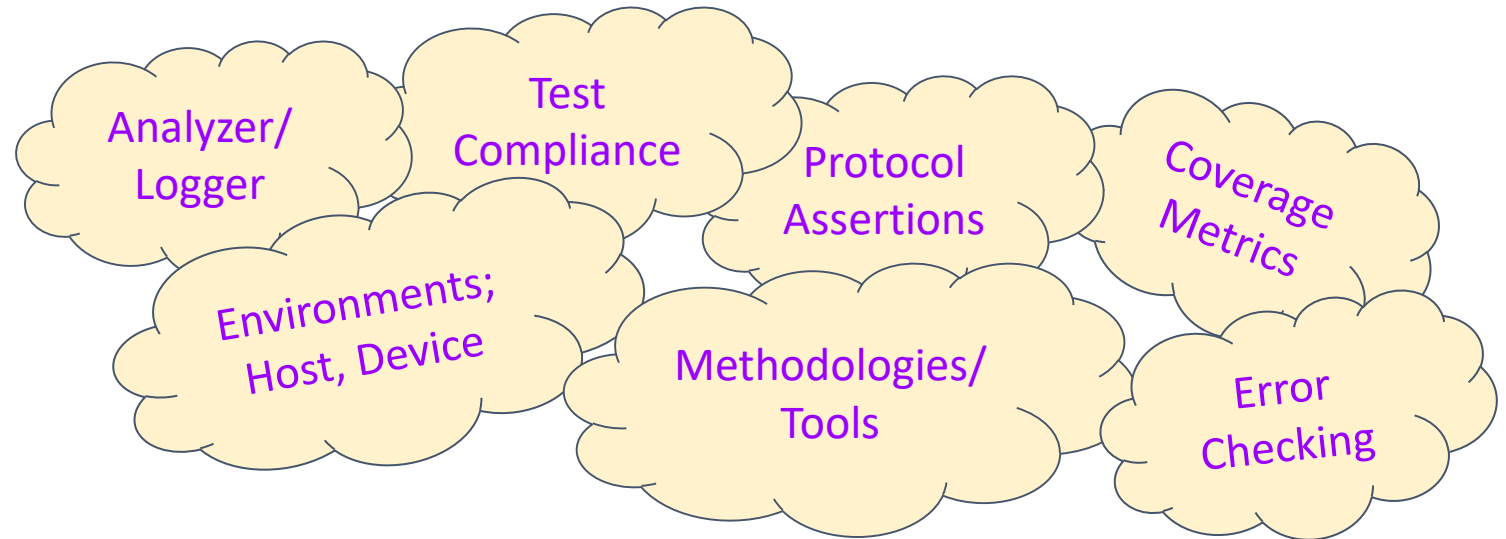Testcase development

Debug mechanisms

Objectives of Verification IP

❏ Rapid Environment Configuration

❏ Ready to use environment

❏ Minimizing time sinks in protocol verification

❏ VIP Performance

❏ Protocol Analyzers

Growing Verification Challenge

Analyzer/ Logger

Test Compliance

Protocol Assertions

Coverage Metrics

Environments; Host, Device

Methodologies/ Tools

Error Checking

❑ Demanding Advanced Functionality, High Performance, Greater Power Efficiency with low cost.

Flexible Configuration: GUI Feature

High-Speed USB Dual-Role Controller Configuration

USB Transceiver Macrocell Interface

Enable Vendor Control Registers: ☐   VControl width (1-32 bits): 4   VStatus width (1-32 bits): 8

Point-to-Point solution or Full Multipoint capablity

Multipoint ☑

Number of DMA channels

● 0   ○ 1   ○ 2   ○ 3   ○ 4   ○ 5   ○ 6   ○ 7   ○ 8

Enable Dynamic FIFO Sizing ☐

Total RAM Size (bytes):   ○ 128   ⊙ 256   ○ 512   ○ 1K   ○ 2K   ○ 4K   ○ 8K   ○ 16K   ○ 32K   ○ 64K

Tx Endpoints

Number of Tx endpoints (in addition to endpoint 0):
○ 1   ○ 3   ○ 5   ○ 7   ○ 11   ○ 15

Enable support for Tx bulk packet splitting: ☐   Enable support for high bandwidth Tx ISO endpoints: ☐

Tx Endpoint 1   ◀   ▶

FIFO Size (bytes):   ○ 8   ○ 16   ⊙ 32   ○ 64   ○ 128   ○ 256   ○ 512   ○ 1024   ○ 2048   ○ 4096   ○ 8192

Share FIFO with Rx endpoint 1: ☐

Rx Endpoints

Number of Rx endpoints (in addition to endpoint 0):
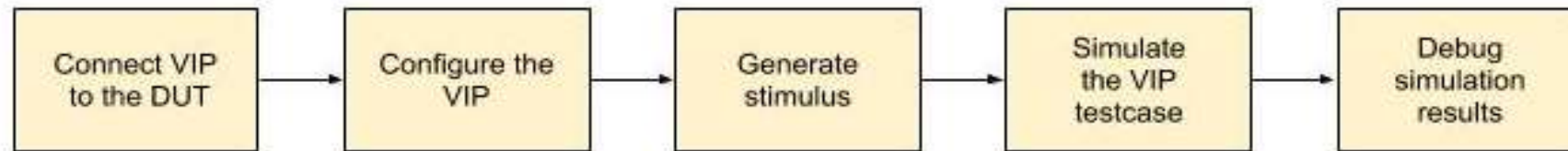○ 1   ○ 3   ○ 5   ○ 7   ○ 11   ○ 15

Enable support for Rx bulk packet combining: ☐   Enable support for high bandwidth Rx ISO endpoints: ☐

Rx Endpoint 1   ◀   ▶

FIFO Size (bytes):   ○ 8   ○ 16   ⊙ 32   ○ 64   ○ 128   ○ 256   ○ 512   ○ 1024   ○ 2048   ○ 4096   ○ 8192

❏ Let user not spend much time in removing compilation warnings once the core is instantiated.


```
ncvlog: *W,MACNDF (-DEFINE macro,1|18): The text macro 'USB_SS_USE_HOST_DB' has also been defined on the command line using the
-DEFINE command line option.  The compiler will ignore the definition found in the Verilog source code.
USB_SS_USE_HOST_DB

ncvlog: *W,TSNSPK (/tools/mnt_tools1/tools1/VIP_10_6a_1_20170620/sv/mvc_pkg.sv,12|14): `timescale is not specified for the package.
The default timescale of 1ns/1ns will be assumed for this package.

ncvlog: *W,FUNTSK (../sequence_lib/usb_ss_bulk_out.svh,36|30): function called as a task without void'().
(`include file: ../sequence_lib/usb_ss_bulk_out.svh line 36, file: ../sequence_lib/sequence_pkg.sv line 13)
          std::randomize(data_payload) with {data_payload.size() == length;}; //RANDOM

ncvlog: *W,NOINUF (/mnt/mnt_tools1/tools1/VIP_10_6b_1_20171002/examples/USB3_0_SS/link_compliance_pkg.sv,31|29):
`include directive not isolated on its own line [16.5(IEEE)].
`include "hdr_pkt_retransmission.svh";
```

Simulation: Aware Protocol Configuration !!

❏ This feature stops the simulation for an invalid configuration and hence saves much simulation time.

```
            Simulation timescale:    1ps
        Writing initial simulation snapshot: worklib.musbmhdrc_dmaint_randp:v
ncsim: 14.10-s014: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Loading snapshot worklib.musbmhdrc_dmaint_randp:v ..................... Done
ncsim> source /var/tools/INCISVE14_10_014/tools/inca/files/ncsimrc
ncsim> run
        0 This configuration is not applicable; One DMA Required. 39
        0    TEST,                                     musbmhdrc_dmaint_rand ; Configuration NOT Applicable
        0    CNA_CNA_CNA
Simulation complete via $finish(1) at time 0 FS + 0
./musbmhdrc_func_gen.v:2546    $finish;
ncsim> exit
```

```
ncsim: 14.10-s014: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Loading snapshot worklib.musbmhdrc_hsm_bulkin2:v ..................... Done
ncsim> source /var/tools/INCISVE14_10_014/tools/inca/files/ncsimrc
ncsim> run
        305 Full-speed Host MP Bulk IN Start

Unable to run Full-speed Host MP Bulk IN as Configuration does not support this test
        305    TEST,                               Full-speed Host MP Bulk IN ; Configuration
        305    CNA_CNA_CNA
Simulation complete via $finish(1) at time 317810 PS + 2
./musbmhdrc_func_gen.v:2546    $finish;
ncsim> exit
```
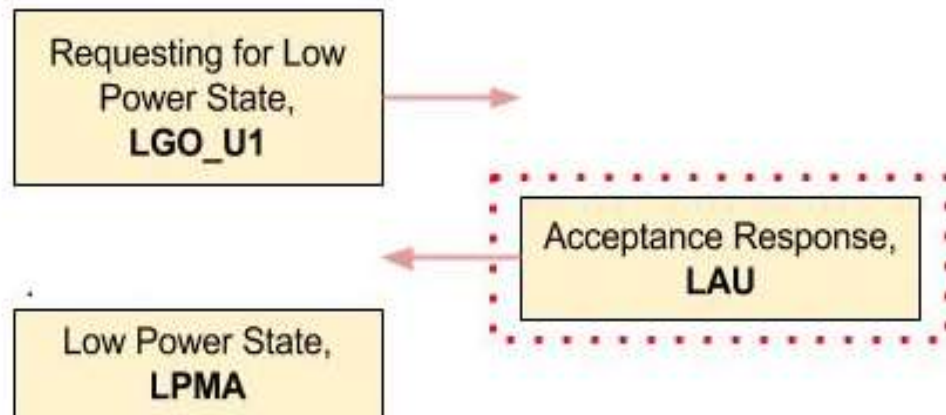
Quicker in Link Bring-Up

❏ Active Enumeration
Host runs read and write transfers to access all descriptor values.

❏ Backdoor Enumeration
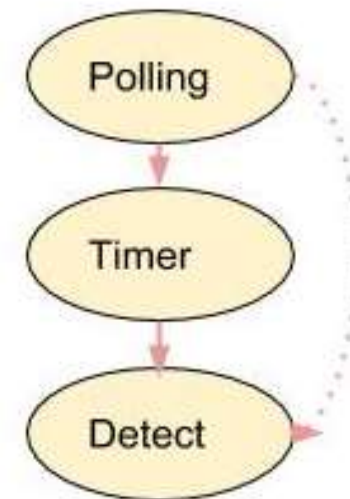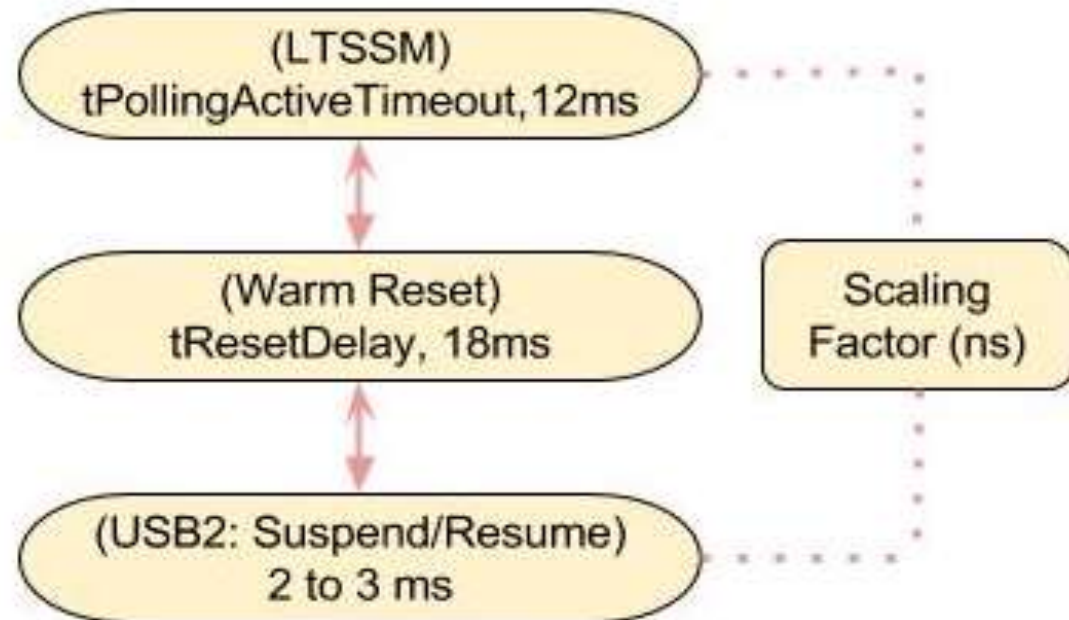USB configuration process happens in zero simulation time.

Fine-Grained Control on Link States
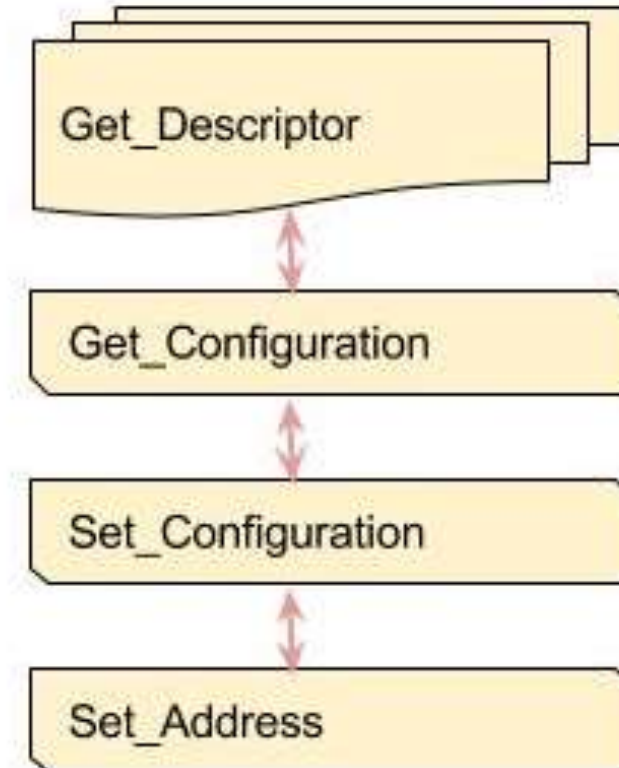
❏ Controlling Link Layer Response
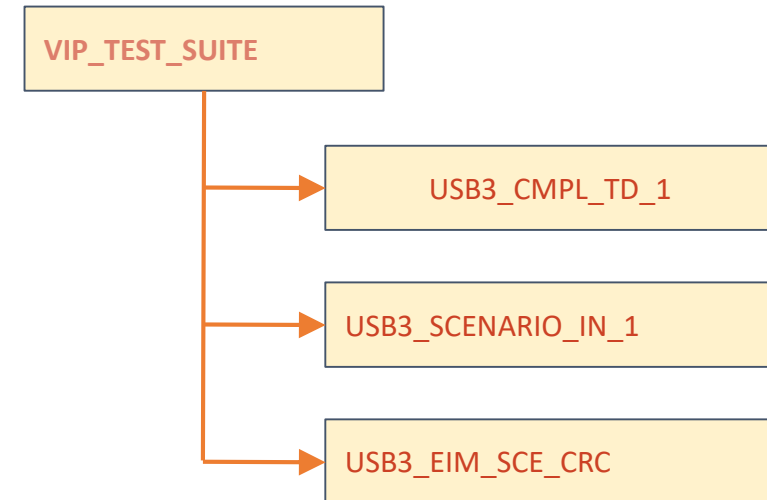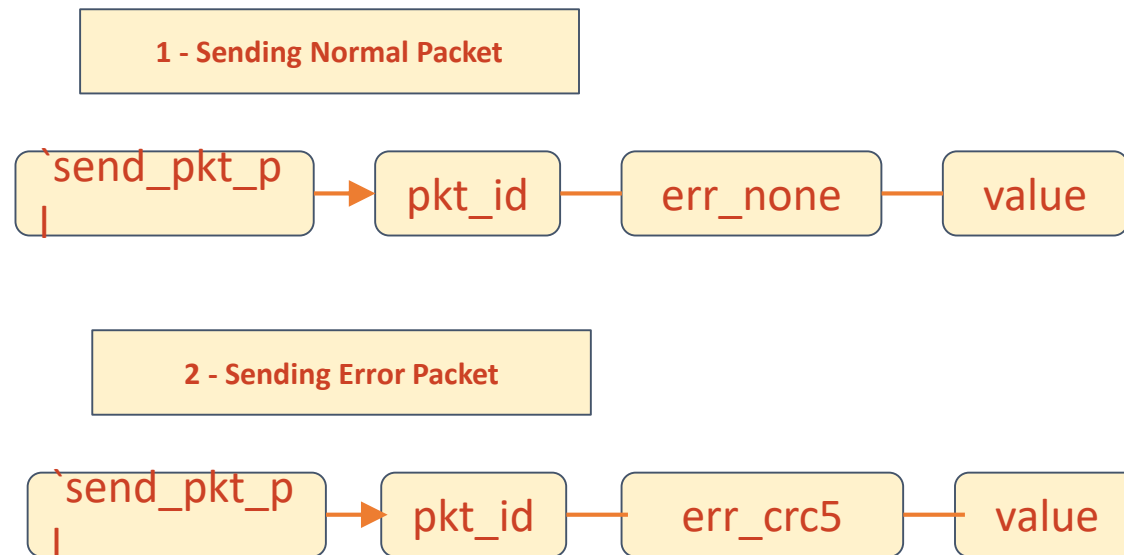
❏ Skips the regular link transition without timeout.

Timing Standardization

❏ `ifdef SIMULATION_VALUE
All timing values follows standard prescribed specification.

❏ `ifdef SIMULATION_SHORT
All timing values are shortened to improve simulation time.

(LTSSM)
tPollingActiveTimeout,12ms

(Warm Reset)
tResetDelay, 18ms

Scaling
Factor (ns)

(USB2: Suspend/Resume)
2 to 3 ms

Testcase Development

1. Grouping Testcases.
2. Highlighting specific information in testcase.
3. Easier APIs for further enhancement.

VIP_TEST_SUITE

USB3_CMPL_TD_1

USB3_SCENARIO_IN_1

USB3_EIM_SCE_CRC

1 - Sending Normal Packet

`send_pkt_pl → pkt_id — err_none — value

2 - Sending Error Packet

`send_pkt_pl → pkt_id — err_crc5 — value

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Running Testcase

- ❏ Built in run script helps user to run testcase with multiple options.

- ❏ Flexibility to user in dumping the results.

run_script

single testcase — multiple testcase — list_file

logger name_1 — log_debug_2

regression option
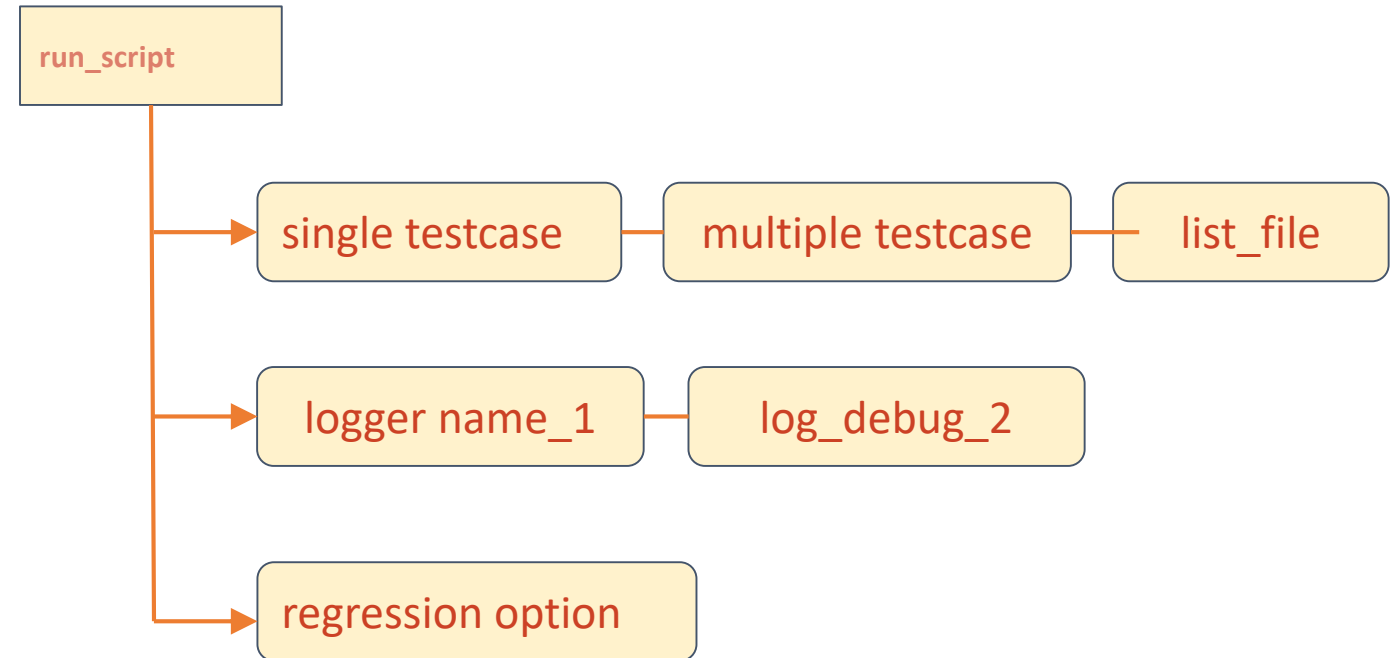
When something went wrong - Debug it 😊

Keep searching for CRC Error ?

❏ Difficulty in identifying error

❏ Easy to recognize the error

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VIPs key thing: Checking for Protocol Violations

❏ Assertion just defines the error

```
ncsim: *E,ASRTST (../src/bus_drv/axi/Axi4PC.sv,3436): (time 767710354 PS) Assertion Axi4PC.axi4_errs_bresp_all_done_eos has failed
AXI4_ERRS_BRESP_ALL_DONE_EOS: All write transaction addresses must have been matched with corresponding write response.
ncsim: *E,ASRTST (../src/bus_drv/axi/Axi4PC.sv,3444): (time 767710354 PS) Assertion Axi4PC.axi4_errs_rlast_all_done_eos has failed
AXI4_ERRS_RLAST_ALL_DONE_EOS: All outstanding read bursts must have completed a the end of the simulation.
Simulation complete via $finish(1) at time 767710354 PS + 0
```

❏ Assertion also refers specification section and sub-section

```
MVC_ERROR @ 7200 ps: (USB3.0-60460) /top/phy_host/usb_ss_if monitor_PowerDown_with_LineState: PIPE_NOT_P3_STATE_WHEN_LINK_IN_SS_DISABLED_U3:1005 -
PowerDown should be P3 when transmitter is in U3 or SS.Disabled link state.
(see PHY Interface For the PCI Express* & USB 3.0 Architectures v3.0 section 6.4)

MVC_ERROR @ 87200 ps: (USB3.0-60448) /top/phy_host/usb_ss_if monitor_signals_during_reset_assertion: PIPE_TX_DEEMP_OTHER_THAN_1_DURING_RESET:969
When reset# is asserted, the MAC should have TxDeemp = 1. (see PHY Interface For the PCI Express* & USB 3.0 Architectures v3.0 section 6.2)
```

Data Checking: Scoreboard

```
60772000    top2_3.i_port3_0.u3_ll_lc.lc_main: LGOOD 3 Received, ADV=0
60772001    mon_pkg::data_monitor.check_data: Initiating HOST CONTROL data checking;len=     8,epnum= 0 Seq_num =
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=00, Actual=00
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=05, Actual=05
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=7c, Actual=7c
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=00, Actual=00
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=00, Actual=00
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=00, Actual=00
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=00, Actual=00
60772001    mon_pkg::data_monitor.check_data: Successful:HOST CONTROL data match for ep 00 Expected=00, Actual=00
60772001     mon_pkg::data_monitor.check_data:Done HOST CONTROL data checking;len=     8,epnum= 0
```

```
UVM_INFO /mnt/tools/mnt_tools1/tools1/QuestaVIP_10_6a_1_20170620/questa_mvc_src/sv/USB3_0_SS/./analysis/usb_ss_device_scoreboard.svh(1871)
usb_ss_host_agent.dev_sb [USB_SS_DEVICE_SCOREBOARD] Data Matched :
Read Data = '{'h12, 'h1, 'h0, 'h3, 'h0, 'h0, 'h0, 'h9, 'h45, 'h0, 'h1, 'h0, 'h1, 'h0, 'h45, 'h1, 'h1, 'h1}
```

```
UVM_ERROR /home/maheshk/projects/QuestaVIP_10_5b_1/questa_mvc_src/sv/USB3_0_SS/./analysis/usb_ss_device_scoreboard.svh(1845) @ 789856800.000 ps
.env.usb_ss_host_agent.dev_sb [USB_SS_DEVICE_SCOREBOARD] Showing Data mismatch at specific indexes:
 At index =        28,
Expected Data = 1
Read Data = 7
```

```
UVM_ERROR /home/maheshk/projects/QuestaVIP_10_5b_1/questa_mvc_src/sv/USB3_0_SS/./analysis/usb_ss_device_scoreboard.svh(1845) @ 789856800.000 ps
.env.usb_ss_host_agent.dev_sb [USB_SS_DEVICE_SCOREBOARD] Showing Data mismatch at specific indexes:
 At index =        29,
Expected Data = 0
Read Data = 7
```

Transaction Logger

Feature: Filtering Protocol Sequences/Patterns

```
822212000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
832230000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
832236000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
842260000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
842260000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
852280000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
852284000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
862310000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
862316000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
872340000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
872340000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
882360000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
882364000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
892390000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
892396000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
902420000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
902420000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
912440000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
912444000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
922470000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
922476000    top_sshost.u3_pkt.lc_tx_req: LUP        submitted for transmission
932500000    top_sshost.u3_ll_ltssm.lc_tx_req: lc = 400
```

```
2635477000    DUT: TS1
2635509000    DUT: TS1
2635527000     TB:  TSEQ
2635541000    DUT: TS1
2635573000    DUT: TS1
2635591000     TB:  TSEQ
2635605000    DUT: TS1
2635637000    DUT: TS1
2635655000     TB:  TSEQ
2635669000    DUT: TS1
2635701000    DUT: TS1
2635719000     TB:  TSEQ
2635733000    DUT: TS1
2635765000    DUT: TS1
2635783000     TB:  TSEQ
2635797000    DUT: TS1
2635829000    DUT: TS1
2635847000     TB:  TSEQ
2635861000    DUT: TS1
2635893000    DUT: TS1
2635911000     TB:  TSEQ
2635925000    DUT: TS1
2635957000    DUT: TS1
2635975000     TB:  TSEQ
2635989000    DUT: TS1
2636021000    DUT: TS1
2636039000     TB:  TSEQ
2636053000    DUT: TS1
2636085000    DUT: TS1
2636103000     TB:  TSEQ
2636117000    DUT: TS1
```

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❏ This helps to know about current Environment Configuration.

❏ Also prints the particular LTSSM state transition.

```
================DEBUG : UPSTREAM LINK================================================
Upstream LinkState is :USB_SS_Disabled
To Exit from this state, g_directed_to_Rx_detect[1] is required to be set
Once this bit is asserted, it will wait for power_down signal to change to P2, which is
acknowledged by Phy through assertion of Phystatus. Once these events occur, the LTSSM state
transition to USB_SS_Rx_Detect_Reset state/substate
--------------------------------------------------------------------------------------

================DEBUG : DOWNSTREAM LINK==============================================
Downstream LinkState is :USB_SS_Rx_Detect
Downstream LinkSubstate is :USB_SS_Rx_Detect_Reset

In this state, it will wait for Warm Reset to be completed if it has transitioned to this state due to detection of Warm Reset,
Else it will transition to USB_SS_Rx_Detect_Active LTSSM state/substate if g_directed_to_SS_Disabled is set to 1'b0
================DEBUG : DOWNSTREAM LINK==============================================
Downstream LinkState is :USB_SS_Polling
Downstream LinkSubstate is :USB_SS_Polling_LFPS

QVIP will generate Polling LFPS signal (tBurst) of 0x000002BC time
Polling LFPS generation time is calculated as usb_ss_Polling_LFPS_tBurst_gen_apply.
usb_ss_Polling_LFPS_tBurst_gen_apply should lie in the range of usb_ss_Polling_LFPS_tBurst_min usb_ss_Polling_LFPS_tBurst_max.

QVIP will generate Polling SCD signal logic 0 (from DUT) of tRepeat value 0x00001B58
QVIP will generate Polling SCD signal logic 1 (from DUT) of tRepeat value 0x00002EE0
Refer to section 7.5.4.3.2 of USB3.1 specification for exit condition from this state using LFPS signaling.
================================================================================
```

Conclusion

- ❏ Non-Protocol experts must also use VIP

- ❏ Fine Tuning is important rather than additional features

- ❏ VIPs are called Plug-And-Play Devices

- ❏ Standard compliant

Questions ?